ABSTRACT

A software programmable DSP with a field programmable instruction set is described where customized instructions can be created, or certain existing instructions can be modified, at the user's location after taking delivery of the processor. The FPGA fabric used to implement the reprogrammable instructions is restricted to supporting the software-programmable DSP - never functioning as an independent coprocessor - and therefore enabling the reprogrammable instructions to exist in the normal stream of DSP software execution. DSP-type functions implemented in the FPGA fabric are also restricted to being automatically generated such that they are synchronous with the processor clocks - enabling easy conversion to an ASIC. Designs implemented on a die containing a DSP with an FPGA-style reprogrammable instruction fabric may be migrated to a smaller die within a family of DSP die containing hard-wired ASIC instruction fabrics, all members of this ASIC family having common I/O functionality to enable operation in the same system socket.

Robert Osann, Jr., 10494 Ann Arbor Ave., Cupertino, CA 95014, 408-313-1990, Bob@Osann.com